H·A

Notice of Allowability	Application No.	Applicant(s)	
	10/776,778	BHATTACHARYA ET AL.	
	Examiner	Art Unit	
	Anjan K. Deb	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 06/24/2005*.

2. ☒ The allowed claim(s) is/are *1-22*.

3. ☒ The drawings filed on *31 March 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Anjan K Deb
Primary Examiner
Art Unit: 2858

DETAILED ACTION

1. This office action is in response to amendment filed 06/24/2005.

Allowable Subject Matter

2. Claims 1-22 are allowed.

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

The primary reason for allowance of the claims 1-11, 15-19 is the inclusion of the detection circuit configured to generate an output signal being at a first logic value indicating that the second voltage supply is substantially at a first voltage level, and output signal being at a second logic level indicating second voltage supply being at a second voltage level, wherein when the second voltage supply is at one of the first and second voltage level, detection circuit draws substantially no current.

The primary reason for allowance of the claims 12-14, 20-22 is the inclusion of the detection circuit wherein the detection circuit is configured to generate an output signal at the output of the detection circuit, wherein the output signal being at a first value indicates that the input signal is substantially at a first voltage level, and wherein the output signal being at a second value indicates that the input signal is substantially at a second voltage level, wherein a

voltage level shift circuit comprises a second transistor, the second transistor including a first terminal connected to the first terminal of the at least one transistor, the second transistor including second and third terminals connected to the first voltage supply of the detection circuit, and a second passive load connected between the first terminal of the second transistor and the second voltage supply.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Higgins et al. (US 3,806,915) discloses (Fig. 4) voltage level detection circuit comprising at least one transistor 42, including a first bias terminal connecting to the first voltage (+) supply, a control terminal 40 for receiving the second voltage supply (ANALOG INPUT), and a third second bias terminal operatively coupled to an output of the circuit (44,50,51, 56, BINARY OUTPUT) and a passive load 48 connected between the third second bias terminal of the at least one transistor 42 and a third voltage supply (-), wherein the detection circuit is configured to generate an output signal (BINARY OUTPUT) at the output of the circuit.

Higgins did not explicitly disclose detection circuit is configured to generate an output signal being at a first logic value indicating that the second voltage supply is substantially at a first voltage level, and output signal being at a second logic level indicating second voltage supply being at second voltage level. While Higgins disclosed that the detection circuit 51 draws substantially no current at the logic level 1 (transistor cut-off) it did not disclose that the detection circuit 51 draws substantially no current at the logic level 0.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Anjan K. Deb whose telephone number is 571-272-2228. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lefkowitz Edwards can be reached at 571-272-2180.

Anjan K. Deb
Primary Patent Examiner
Art Unit: 2858
8/18/05

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